

AIC111EVM

User's Guide

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM with an input voltage of 3.3 V and the output voltage range of 0.9 V to 2.5 V, or an input voltage of 5 V and the output voltage range of 0.9 V to 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Read This First

About This Manual

This user's guide describes the operation and use of the AIC111 codec. A complete circuit description as well as a schematic diagram and bill of materials are also included.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—Introduction
- Chapter 2—Digital Interface
- Chapter 3—Analog Interface
- Chapter 4—AIC111 Bill of Materials and Schematic

Related Documentation From Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, please identify this booklet by its title and literature number. Updated documents can also be obtained through our website at www.ti.com.

Data Sheets:

AIC111
SN74AUC1G125

Literature Number

SLAS382
SCES382F

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This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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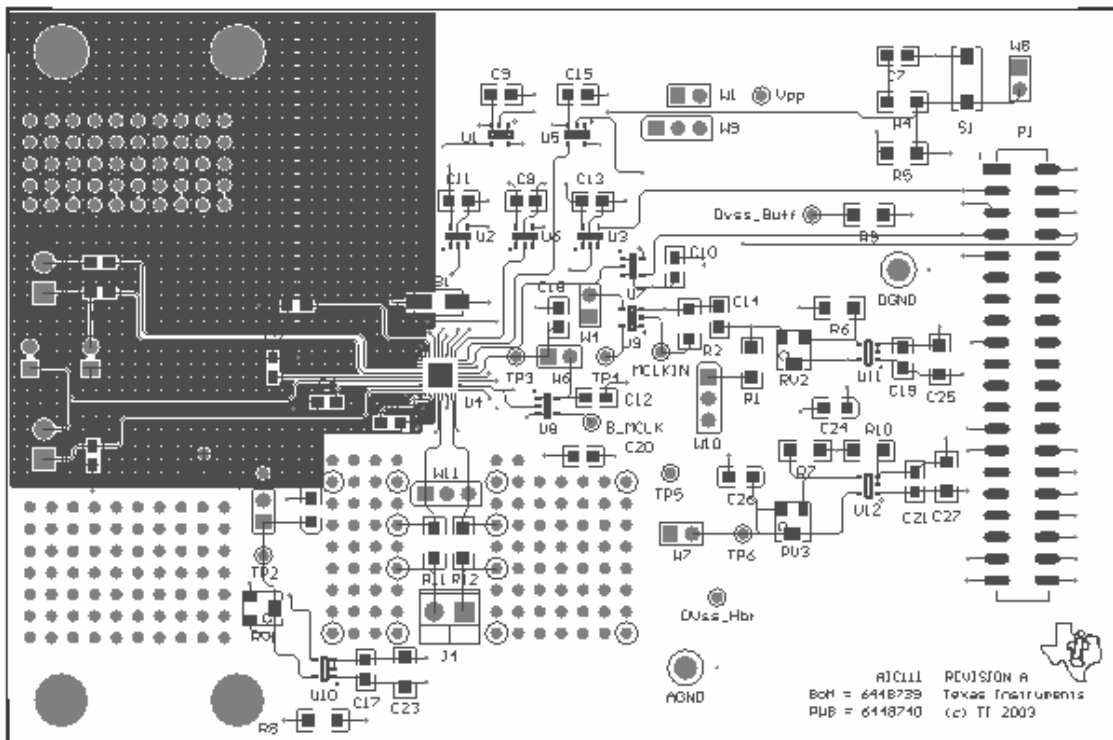
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Introduction

This user guide provides support for the AIC111 device.

The AIC111 features a $\Delta\Sigma$ ADC & DAC, a programmable time-constant PGA/compressor interface, and a glueless interface to many DSPs.

The device featured on the EVM is a 5x5 QFN (quad flatpack no leads)



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Digital Interface

The digital signals required to operate this codec originate from the 40-pin connector – J1. There are two methods to drive the digital interface:

- Create a custom interface between the codec EVM and the host system.
- Alternatively, if a TI DSK (DSP starter kit) is the host system, a development platform is available from TI. This platform provides the additional functions that the codec requires in a convenient form factor.

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2.1 Codec-to-Platform

The AIC111 mates with the development platform via a 40-pin Samtec connector. The mating connector (Samtec part number, TSM-120-01-T-DV-P) is used on the development platform to provide the electrical connections necessary. Consult Samtec at www.samtec.com or 1-800-SAMTEC-9 for more information.

The pinout for the 40-pin connector is given below.

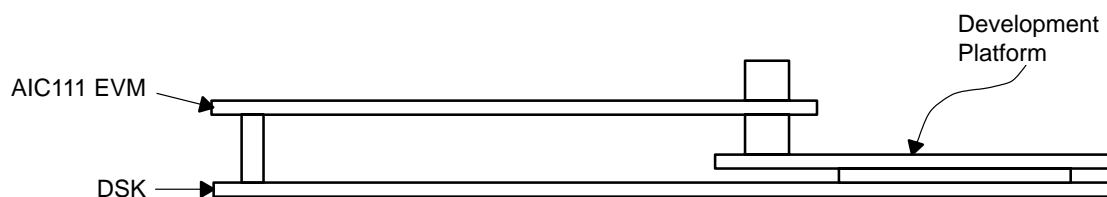
Pin Number	Signal	Description
J1.1	Not used	
J1.2	DGND	Digital ground
J1.3	SCLK	Serial data clock
J1.4	DGND	Digital ground
J1.5	DIN	Data in
J1.6	DGND	Digital ground
J1.7	DOUT	Data out
J1.8	LBM	Low battery monitor
J1.9	Not used	Frame sync
J1.10	Not used	
J1.11	Not used	
J1.12	Not used	
J1.13	Not used	
J1.14	Not used	
J1.15	Not used	
J1.16	Not used	
J1.17	Not used	
J1.18	Not used	
J1.19	Not used	
J1.20	Not used	
J1.21	Not used	
J1.22	Not used	
J1.23	Not used	
J1.24	Not used	
J1.25	3.3V_D	Digital 3.3 V
J1.26	Reserved	Reserved for future use
J1.27	3.3V_D	Digital 3.3 V
J1.28	DGND	Digital ground
J1.29	Not used	
J1.30	DGND	Digital ground
J1.31	Not used	
J1.32	DGND	Digital ground
J1.33	Not used	
J1.34	AGND	Analog ground
J1.35	Not used	
J1.36	AGND	Analog ground
J1.37	3.3V_A	Analog 3.3 V
J1.38	AGND	Analog ground

Pin Number	Signal	Description
J1.39	3.3V_A	Analog 3.3 V
J1.40	AGND	Analog Ground

The development platform provides a convenient mechanical and electrical interface between the serial port on the DSK and the EVM.

Refer to Ti literature number SLAU090 for details regarding the development platform.

Further descriptions regarding the operation of this EVM assumes that the Development Platform is used. The figure below shows the method necessary to connect the DSK to the development platform, and the development platform to the codec.



2.2 Jumper Options

There are various jumpers on the board that can be configured in a variety of ways, depending upon the user's requirements. Their functions are briefly presented below:

Jumper	Function	
W1	Reserved, never install a jumper at this location	Never install
W2	Supplies bias voltage for AVIN_P, if required	Not installed
W3	Grounds AVIN_M, for single-ended input, if required.	Not installed
W4	Reserved, never install a jumper at this location	Never install
W5	Completes the connection for the codec's analog and core digital supplies. – remove this jumper and place a current meter between TP1 and TP2 to check current drawn.	Installed
W6	Completes the connection for the codec's digital I/O supply. – remove this jumper and place a current meter between TP3 and TP4 to check current drawn.	Installed
W7	Completes the connection for the codec's digital H-bridge supply – remove this jumper and place a current meter between TP5 and TP6 to check current drawn.	Installed
W8	When inserted, the device is permanently reset.	Not installed
W9	Reserved, never install a jumper at this location	Never install
W10	Selects the digital interface	Install between pins 2 and 3
W11	Input for add-on conditioning board	Never install
P1.32–P1.34	Connect AGND and DGND together	Installed

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Analog Interface

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3.1 Input Connections

Analog input is via a screw terminal – J2. The input can be single ended or differential.

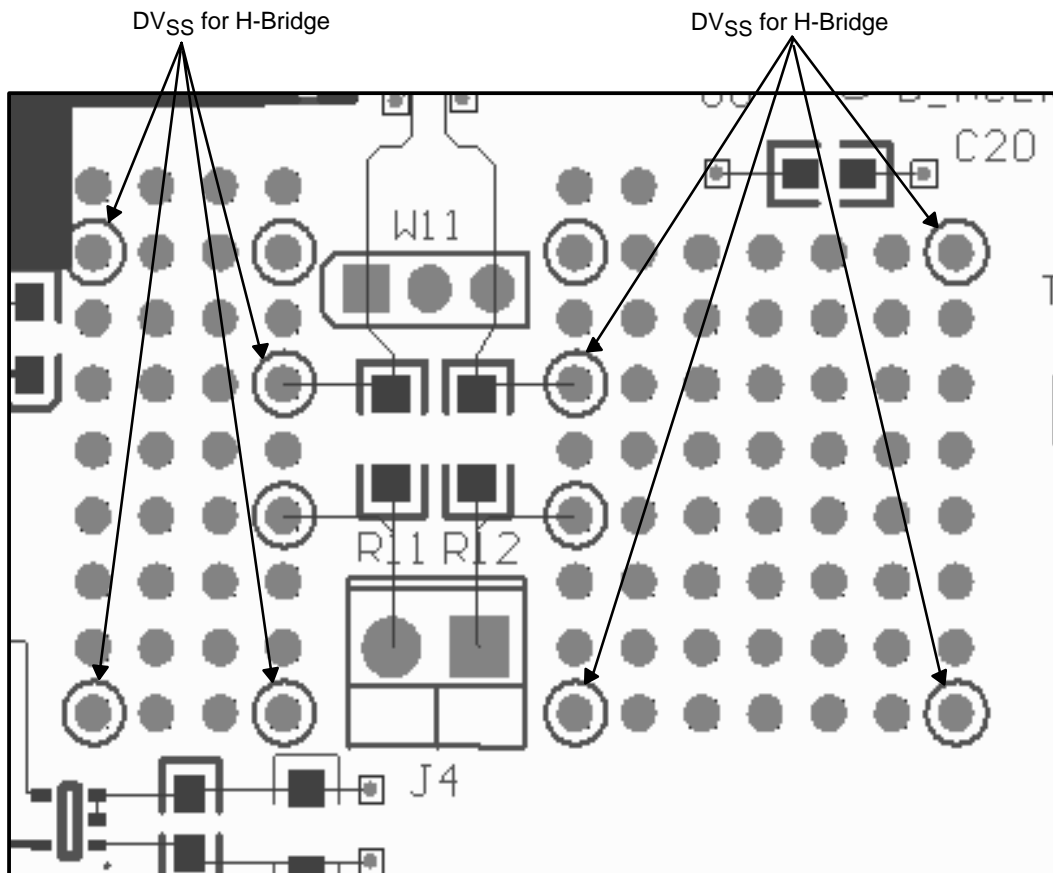
Bias current and voltage for an external microphone is provided via a screw terminal – J3.

3.2 Output Connections

The output from the AIC111 is from an H-bridge driver. These output topologies generally require a filter to recover the analog output signal. The output signal is available at J4.

The prototype area on the EVM can be used to build a simple filter, or alternatively, it is possible to build a small conditioning board which fits on top of the prototype area. Check with the factory for availability of filter boards.

Convenient points for picking-up the H-bridge ground are located around the prototype area and are indicated on the silkscreen by circles around the plated through holes.



Bill of Materials and Schematic

The bill of materials and schematic for the AIC111EVM are provided in this chapter.

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4.1 Bill of Materials

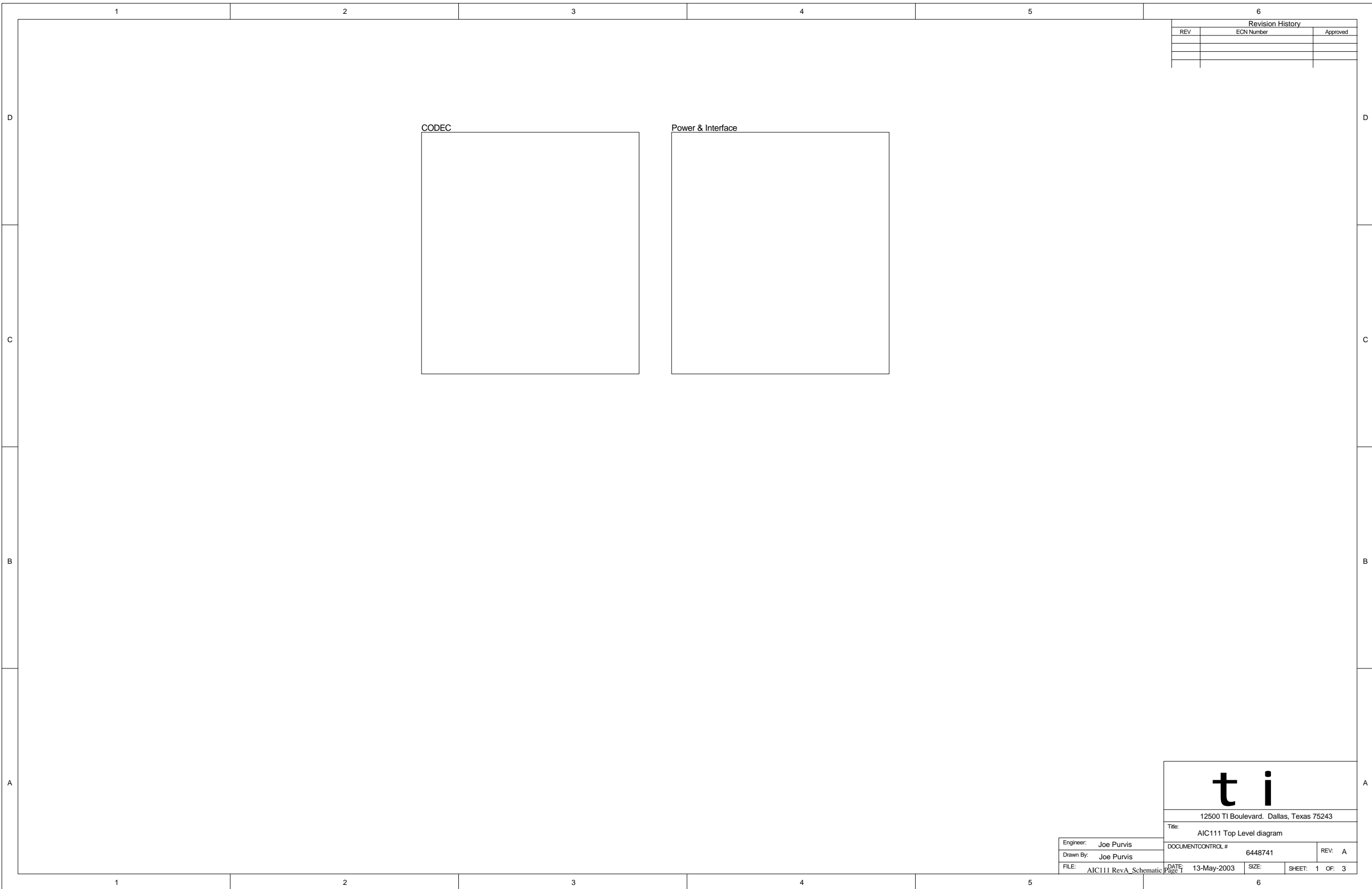
The following table contains a complete Bill of Materials for the AIC111EVM. The schematic diagram is also provided for reference. Contact the Product Information Center or e-mail dataconvapps@list.ti.com for questions regarding this EVM.

Used	Value	Ref Des	Description	Vendor	Part Number
6	0R	R1 R8 R9 R10 R11 R12	Resistor 0 Ω 1/8W 5% 1206 SMD	Panasonic	ERJ-8GEY0R00V
1	10K	R2	Resistor 10 k Ω 1/8W 5% 1206 SMD	Panasonic	ERJ-8GEYJ103V
2	61.9K	R6 R7	Resistor 61.9 k Ω 1/8W 1% 1206 SMD	Panasonic	ERJ-8ENF6192V
1	130K	R5	Resistor 130 k Ω 1/4W 5% 1206 SMD	Panasonic	ERJ-8GEYJ134V
2	169K	R3 R4	Resistor 169 k Ω 1/8W 1% 1206 SMD	Panasonic	ERJ-8ENF1693V
3	100K	RV1 RV2 RV3	TRIMPOT 100 k Ω 4MM TOP ADJ SMD	Bourns	3214W-1-104E
3	0.047 μ F	C23 C25 C27	Capacitor 47000 pF 50 V ceramic X7R 1206	Kemet	C1206C473K5RACTU
13	0.1 μ F	C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C18 C20	Capacitor 0.1 μ F 25 V ceramic X7R 0805	Panasonic	ECJ-2YB1H104K
5	1 μ F	C1 C2 C3 C4 C5	Capacitor 1 μ F 10 V Ceramic X5R 0805	Panasonic	ECJ-2YB1A105K
3	4.7 μ F	C22 C24 C26	Solid tantalum capacitor, ESR = 3.5R	Kemet	T494A475(1)006AS
3	NI	C17 C19 C21	*	*	*
1	SM_FB_2773044447	FB1	Fair-Rite SM beads #24--44447	Fair-Rite	2744044447
8	SN74AUC1G125	U1 U2 U3 U5 U6 U7 U8 U9	Single bus buffer with 3-state output	Texas Instruments	SN74AUC1G125DBVR
3	TPS77001	U10 U11 U12	Ultralow power 50-mA LDO regulator	Texas Instruments	TPS77001DBVT
1	AIC111	U4	Codec	Texas Instruments	AIC111
1			PWB	Texas Instruments	6448740
8	2POS_JUMPER	W1 W2 W3 W4 W5 W6 W7 W8	2-position jumper	Samtec	TSW-102-07-L-S
3	3POS_JUMPER	W9 W10 W11	3-position jumper	Samtec	TSW-103-07-L-S
1	40-Pin plug	P1	40-PIN SMT PLUG	Samtec	TSM-120-01-T-DV-P
1	40-Pin socket	J1	40-Pin SMT socket	Samtec	SSW-120-22-F-D-VS-K
3	Screw terminal 2X1	J2 J3 J4	2-pole screw terminal 3,5 mm pitch black	On Shore Technology	ED-555-2-BK

Used	Value	Ref Des	Description	Vendor	Part Number
1	SW-PB	S1	Switch LT TOUCH 6X3.5 240GF SMD	Panasonic	EVQ-PJU04K
12	TP_0.025	AVss B_MCLK DVss_Hbr Dvss_Buff MCLKIN TP1 TP2 TP3 TP4 TP5 TP6 Vpp	Test Point - single 0.025" pin	Keystone Electronics	5000
2	TP_TURRENT	AGND DGND	Turret terminal test point	Cambion	180-7337-02-05
5			Shunt	Samtec	SNT-100-BK-T
2			1.000/4-40 nylon hex thread SP	Keystone Electronics	1902E
2			4-40 X 1/4 machine screw PH SS	Building Fasteners	PMSSS 440 0025 PH

4.2 Schematic

The schematics are shown on the following pages.

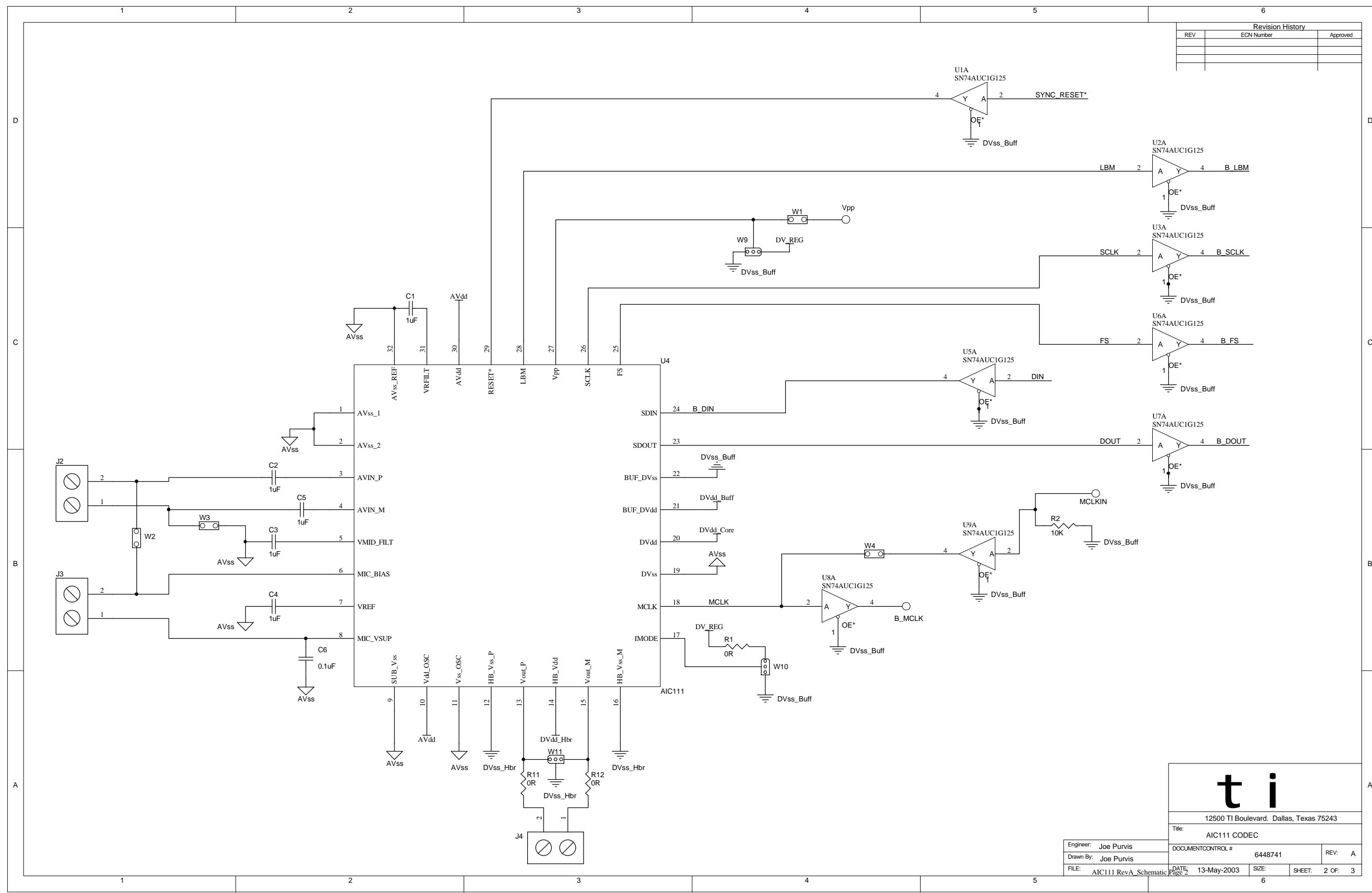


Revision History		
REV	ECN Number	Approved

ti		
12500 TI Boulevard, Dallas, Texas 75243		
Title: AIC111 Top Level diagram		
Engineer: Joe Purvis	DOCUMENT CONTROL # 6448741	REV: A
Drawn By: Joe Purvis	DATE: 13-May-2003	SIZE: SHEET: 1 OF: 3

Engineer: Joe Purvis	DOCUMENT CONTROL # 6448741	REV: A
Drawn By: Joe Purvis	DATE: 13-May-2003	SIZE: SHEET: 1 OF: 3

Revision History		
REV	ECN Number	Approved



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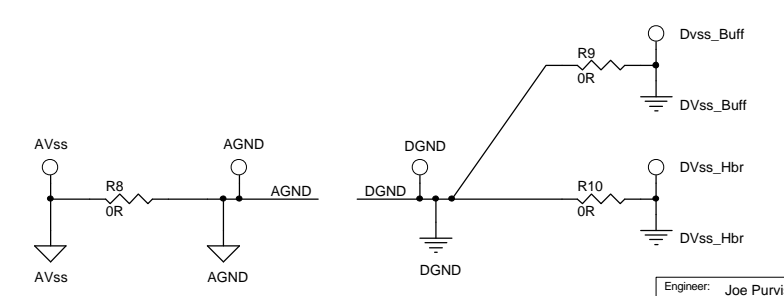
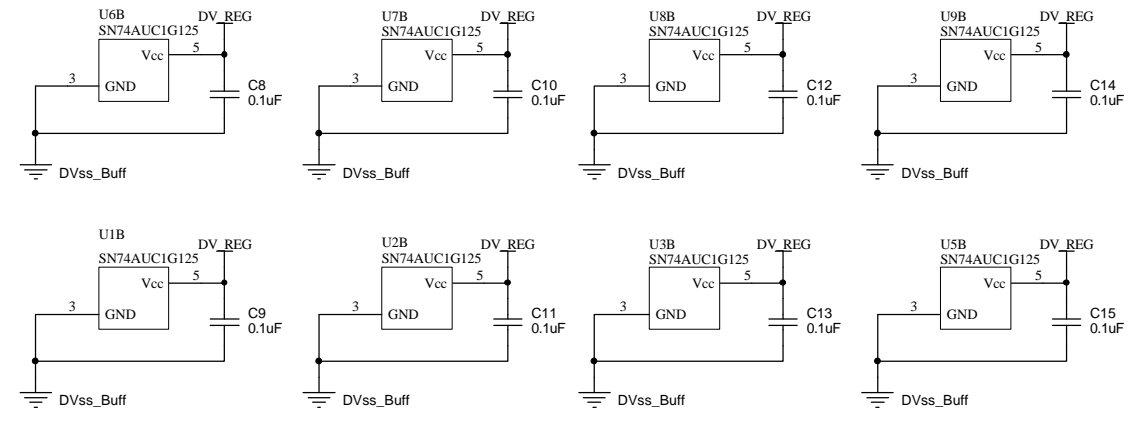
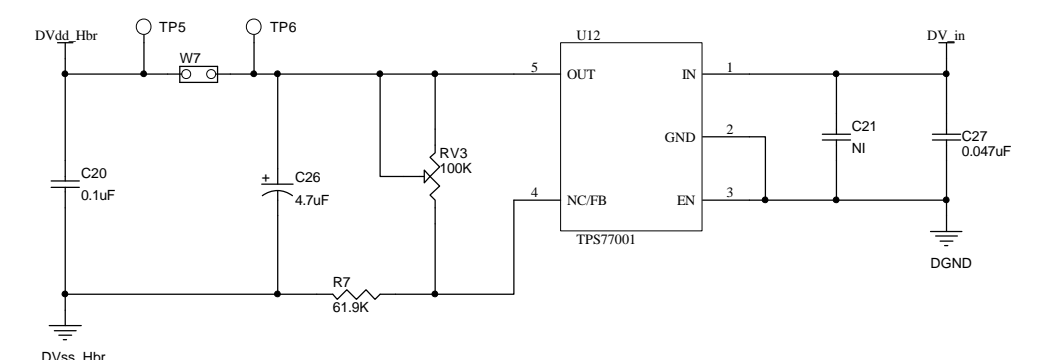
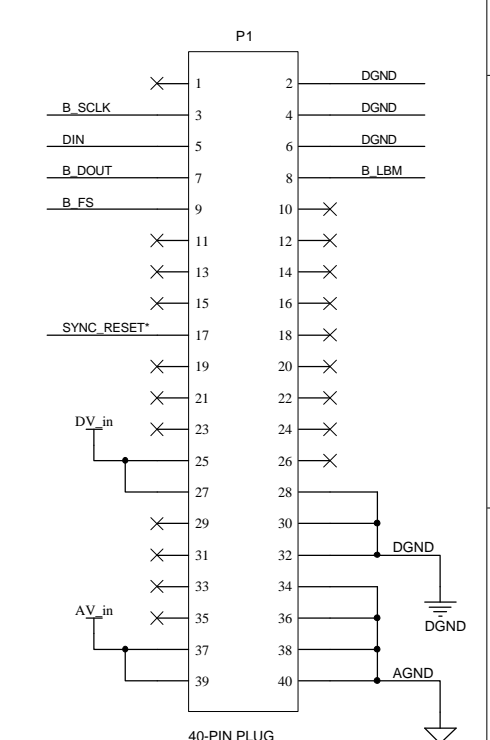
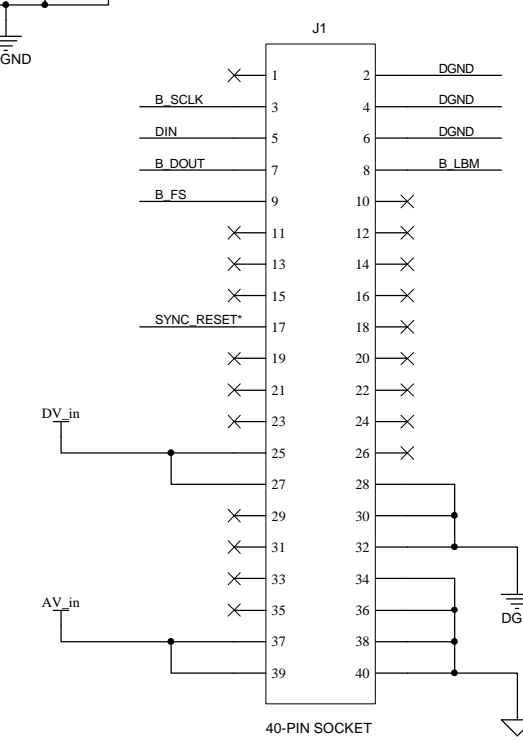
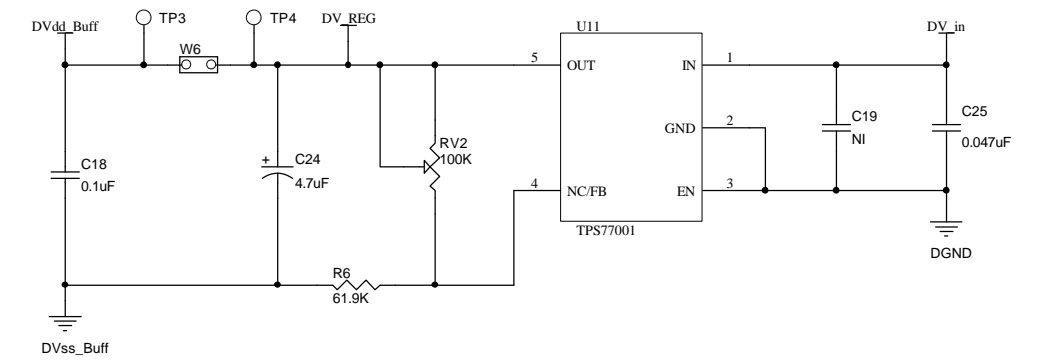
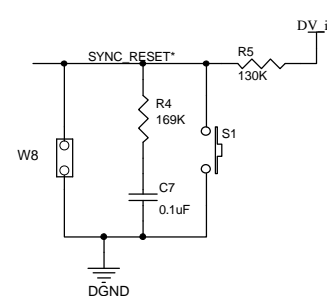
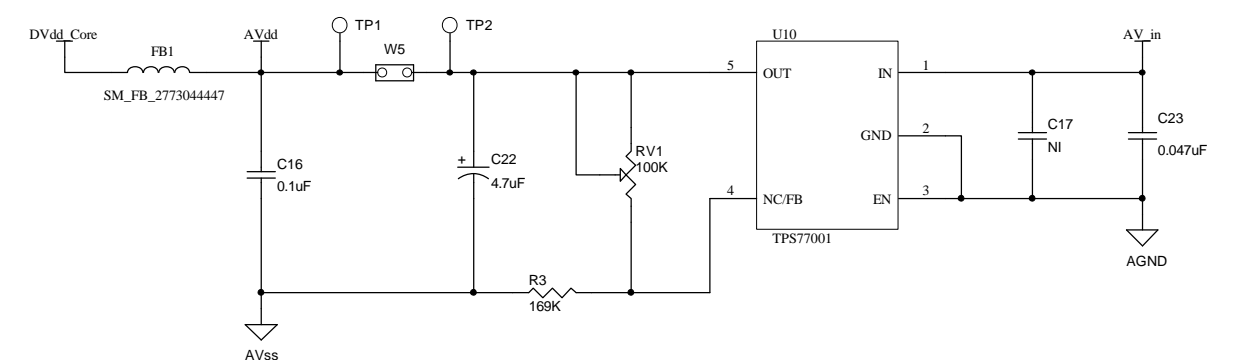
Title: AIC111 CODEC

Engineer: Joe Purvis DOCUMENT CONTROL # 6448741 REV: A

Drawn By: Joe Purvis

FILE: AIC111 RevA Schematic Page 2 DATE: 13-May-2003 SIZE: SHEET: 2 OF 3

Revision History		
REV	ECN Number	Approved



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Title: AIC111 DSP Interface & Power

DOCUMENT CONTROL # 6448741 REV: A

Engineer: Joe Purvis
 Drawn By: Joe Purvis
 DATE: 13-May-2003
 FILE: AIC111 RevA Schematic Page 3

SIZE: SHEET: 3 OF: 3